33. (Once Amended) A microcomputer according to claim 32,

wherein the memory which stores the write control program is a RAM that receives the write control program from the ROM.

34. (Not Amended) A microcomputer according to claim 31, further comprising:

a data bus to which the central processing unit, the input and output unit, the ROM and the memory are coupled; and

an address bus to which the central processing unit, the input and output unit, the electrically programmable ROM and the memory are coupled.

REMARKS

Claims 31-34 remain pending. Claims 31, 32 and 34 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Ugon, U.S. Patent No. 4,382,279; and claim 33 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over the Ugon reference. Reconsideration of the rejections is requested in view of the foregoing amendments and the following remarks.

Claims 31 -34 are directed to a microcomputer on a semiconductor chip that includes an electrically erasable and

programmable ROM capable of storing a program and data. Claim 31 has been amended to clarify the relationship between the program and the write control program. That is, claim 31 now sets forth that the program to be stored in the electrically erasable and programmable ROM is a first program and the write control program that includes an instruction which changes a process of the central processing unit is a second program.

Claim 31 is supported by the description of the invention set forth on page 9, line 30 to page 10, line 5 of the specification, which states that:

> the write operation of the user program may be effected by a construction wherein the CPU 1 receives a program from the outside through the I/O unit 5 in accordance with the program of mask ROM 3, and then makes the write operation to the user program region M1 of EEP-ROM 4.

Since such an operation does not allow direct access to the built-in EEP-ROM 4 from the outside, security is maintained. Thus, for example, the microcomputer is suitable for a single chip type microcomputer incorporated in an IC card.

According to the present invention, the first program, which may be a user program, and data to be stored in the electrically erasable and programmable ROM is supplied from outside of the semiconductor chip via the input and output circuit. Further, the first program or the data is written

into the electrically erasable and programmable ROM by the central processing unit executing the write control program. That is, the central processing unit controls the write control circuit based on the execution of the write control program. Further, according to the present invention, the first program may be an operation program that can be changed by the central processing unit executing the write control program. Thus, if a program bug is found in the program that has been stored in the electrically erasable and programmable ROM, a revised new program can be programmed into the electrically erasable and programmable ROM after erasing the program with the bug from the electrically erasable and programmable ROM.

The claimed microcomputer on a semiconductor chip may, for example, be a microprocessor with flash memory. In such a case, the flash memory can store the operation program and the data that is supplied from the outside of the microprocessor and the operation program can be programmed into the flash memory by setting an operation mode of the microprocessor into a predetermined programming mode, e.g. a PROM writer programming mode or on-board programming mode. If a program bug is found in the operation program stored in the flash

memory or a new operation program is developed, the reprogramming of the flash memory can be performed.

In Ugon, the disclosed microprocessor architecture includes an EPROM 101, which is relied upon in the Office Action for including a write control circuit that is equivalent to that of the present invention. However, the microcomputer of the invention, which includes the claimed write control circuit and the electrically erasable and programmable ROM of the invention are not disclosed or rendered obvious by the disclosure of Ugon.

Specifically, the reference discloses that:

> In the majority of applications it is possible to construct the program in such a way that memory block M1 contains all the non-evolving programs or parts of programs and block M2 contains the evolving programs or parts of programs. In an application of this kind memory block M1 can be produced in the form of a read-only memory (ROM) to reduce manufacturing costs and the physical area of this part of the memory; in this case there is no longer a write voltage V.sub.p1. The second memory block M2 on the other hand must necessarily be in the form of a PROM or EPROM memory (emphasis added). (See col. 6, lines 1-15 of the reference.)

Further, col. 6, lines 55 to 68 of the Ugon reference discloses that:

> With this architecture, a program which is executed in blocks M1 and M2 of memory 101 modifies the information content of memory block M2. More particularly, if the program is to modify the memory

> content at an address 2FOH (i.e., the 752nd word in the memory) using the result of an operation situated in the accumulator 108, the program stores the address 2FOH beforehand in the working registers R0 and R1 of the set 111.
>
> The automatic programming is performed by a sub-program called "PROG" which is stored in memory block M1. This sub-program PROG needs to perform all the functions required for writing in the memory 101 and, in particular, needs to use sequences which are compatible with the fabrication technology employed (emphasis added).

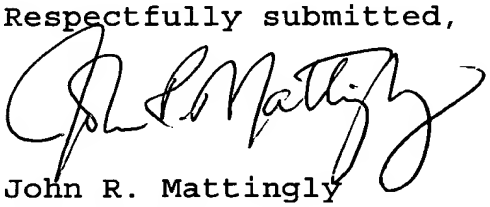
That is, memory Block M1 contains all the non-evolving part of the programs, and memory block M2 contains the evolving part of the programs. The content of memory block M2 is modified by the program that is executed in blocks M1 and M2 of memory 101. Accordingly, one having ordinary skill in the art would consider that the non-evolving part of the program corresponds to an operation program or a data processing program, and the evolving part of the programs corresponds to data that is used by the operation program or data processing program. Accordingly, in the Ugon reference, the non-evolving part of the program in memory block M1 is not clearly disclosed as being modified.

On the other hand, in the present invention, as defined by claim 31, an electrically erasable and programmable ROM is claimed that is capable of storing a first program and data,

and the central processing unit performs a writing to the ROM of the first program or the data from outside of the semiconductor chip via the input and output unit by controlling the write control circuit based on the write control program. Therefore, the Ugon reference does not fairly suggest the invention as claimed by Applicants and therefore claims 31-34 should be found allowable over Ugon and the remainder of the art of record.

In view of the foregoing amendments and remarks, reconsideration and reexamination are respectfully requested.

Respectfully submitted,



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MARKED UP VERSION OF REWRITTEN CLAIMS

31. (Once Amended) A microcomputer on a semiconductor chip, the microcomputer comprising:

a central processing unit;

an electrically erasable and programmable ROM capable of storing a first program and data;

a write control circuit which performs a writing of the first program or the data to the ROM under control of the central processing unit;

a memory in which a second program as a write control program for a writing to the ROM is stored; and

an input and output unit;

wherein the central processing unit performs a writing to the ROM of the first program or the data input from outside of the semiconductor chip via the input and output unit by controlling the write control circuit based on the write control program,

wherein the write control program includes an instruction which changes a process of the central processing unit to a process that controls a writing of the ROM based on the write control program stored in the memory, and

wherein the write control program includes an instruction which returns the process of the CPU to a process based on the program stored in the ROM after completion of the process that controls the writing of the ROM.

32. (Once Amended) A microcomputer according the claim 31,

wherein the memory which stores [a] the write control program is a mask ROM.

33. (Once Amended) A microcomputer according to claim 32,

wherein the memory which stores [a] the write control program is a RAM that receives the write control program from the ROM.

34. (Not Amended) A microcomputer according to claim 31, further comprising:

a data bus to which the central processing unit, the input and output unit, the ROM and the memory are coupled; and

an address bus to which the central processing unit, the input and output unit, the electrically programmable ROM and the memory are coupled.